A MONOLITHIC MULTI-STAGE 6-18 GHz FEEDBACK AMPLIFIER

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ABSTRACT

A design approach and circuit modeling method, which includes parasitic effects, will be presented for a two-stage monolithic feedback amplifier with enhanced high frequency performance. Using the proposed approach, a 6-18 GHz amplifier has been demonstrated with low input/output VSWR, respectable noise figure (6 dB) and a minimum gain of 8 dB.

SUMMARY

The GaAs FET amplifier has become the basic building block of modern microwave systems and as such, usually carries the burden of establishing system bandwidths, sensitivities and dynamic range. These parameters are especially important in ECM and surveillance systems. However, unlike discrete microwave amplifiers, which tend to be bandwidth limited by circuit and assembly techniques, monolithic feedback amplifiers exhibit excellent bandwidth and dynamic range characteristics, and can be directly cascaded. Thus, the size, density and performance of present day EW systems can be enhanced by employing this technology.

Recently, several monolithic feedback amplifiers have been reported with frequency limits of approximately 8 GHz [1,2], but what follows is a method to design monolithic multi-stage feedback amplifiers with high frequency performance extending above 18 GHz. The design and performance of a two-stage 6-18 GHz amplifier aids in the illustration of the proposed technique.

AMPLIFIER DESIGN TECHNIQUES

One of the prime areas of difficulty in designing cascaded MESFET amplifiers is controlling the impedance match between devices [3]. Shunt feedback can be used to reduce the magnitude of S_{11} and S_{22} at the terminals of the active elements, thus enabling the circuit designer to synthesize wideband matching networks. Flat gain versus frequency and greatly improved amplifier stability, especially at lower microwave frequencies, are also desirable byproducts of feedback[4,5]. This improved circuit performance is not without cost; it is obtained at the expense of reduced transducer gain.

In practice, when the feedback element values are lowered to reduce FET maximum available gain, the gain-versus-frequency response begins to exhibit an upward slope. This effect is due to the fact that uniform amounts of negative feedback cannot be applied due to the finite phase shift of the feedback loop and the increasing phase shift of the device as a function of frequency. Hence, there will exist an optimum gain level obtainable with a particular FET and feedback loop circuit.

At frequencies above 14 GHz, the amplifier performance degradation, due to the effects mentioned above, is pronounced. However, a monolithic circuit realization can aid in alleviating some of the drawbacks encountered in hybrid design with extended high-frequency performance. To begin the amplifier design, a monolithic FET model must be developed. This is not an easy task in that S-parameters for monolithic devices are not usually available since direct device measurements must be made. The formulation of the model is further complicated by the fact that an accurate value of the angle of S_{21}, as well as the magnitude, must be known. The FET size is also an important consideration in that the associated feedback loop and input/output matching network element's absolute values are scaled directly with the input and output impedances of the FET.

With the above constraints being considered, a 300-micron, high gain FET with 75-micron-long fingers and 0.5 micron gate length was chosen as the active device. A circuit model for the device includes the source via inductance (Figure 1). The element values for the model were extrapolated from measured S-parameter data of discrete FET's. However, the values of input and output capacitances

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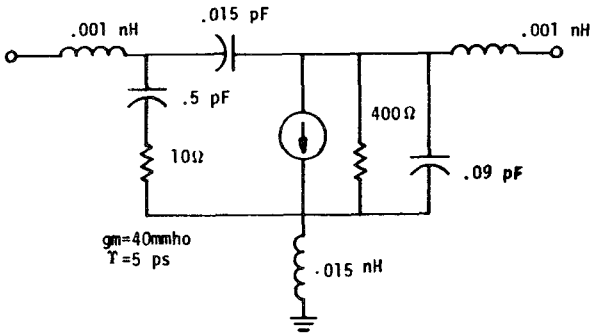

Figure 1. Lumped element 300 μm FET model.

were modified based on geometry differences between the discrete and monolithic devices, and the source lead inductance was changed to account for mounting differences.

Once an appropriate FET model has been chosen, the desired performance of the composite FET and feedback loop can be determined by employing CAD techniques and careful modeling [6]. The input and output networks are now added to complete a single stage design. A typical circuit model is shown in Figure 2.

With a single stage amplifier designed, multistage amplifiers can be constructed by cascading several gain stages. The reduced bandwidth and accentuated gain ripple resulting from directly cascading gain stages can be reduced or eliminated by adjusting the interstage networks (input/output network) to obtain an amplifier with an equal ripple performance. It is not uncommon that the gain and bandwidth of a properly designed two stage amplifier will usually compare favorably with the performance obtained with a single stage design. With larger cascade designs, it may be necessary to design an interstage network that has a completely different ripple characteristic in order to obtain the optimum gain performance.

MONOLITHIC CIRCUIT DESCRIPTION

The above design philosophy was employed in the fabrication of a two stage, monolithic amplifier. The amplifier devices are interdigitated 300 micron FET's which use plated-through source vias to establish RF and DC ground. Vias, with a diameter of 0.084 mm, centered on a 0.2-mm square pad, were chosen in order to minimize the length of the feedback path. All capacitors are of the metal-insulator-metal fabrication type and are used to perform DC blocking as well as RF bypassing functions. Series and shunt resistors in the gate bias circuitry are used to prevent device damage from static and to provide a measure of over-voltage protection. Matching networks of the highpass form were also employed to minimize amplifier length and to provide decoupling for DC bias (gate and drain).

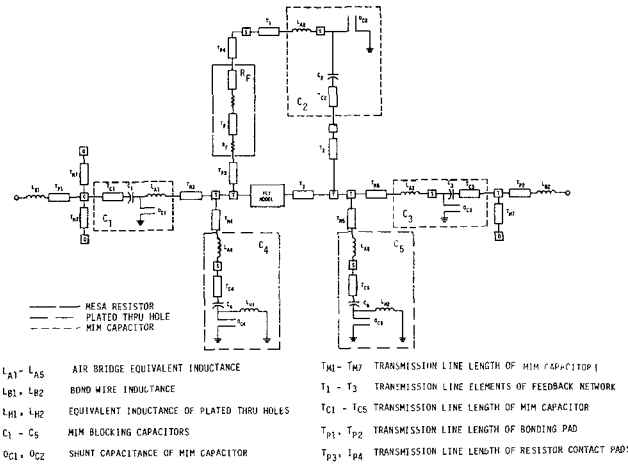

Figure 2. Single-stage amplifier circuit model.

AMPLIFIER CIRCUIT FABRICATION

The two stage feedback amplifier was constructed on a 0.1-mm-thick, semi-insulating, GaAs substrate. The active layers of the circuit have a doping level of approximately 2 X 10^{17} cm^{-3}. The FET source via holes were fabricated using reactive ion etching methods.

The bypass and decoupling capacitors used in the amplifier are of the metal/silicon nitride/metal type, with a 400 nm layer of silicon nitride as the dielectric. With this thickness, the MIM capacitors have about 150 pF/mm^2; thus, 1 pF capacitors are about 80 microns X 80 microns, and 10 pF capacitors are about 250 microns X 250 microns.

The high impedance transmission lines used as inductors in the monolithic amplifier are several skin-depths thick to reduce the resistance as much as possible. In order to produce transmission lines three to four microns thick, extra gold was plated during the air bridge process.

Mesa resistors were used throughout the amplifier and were fabricated during the first photo-etching of the active layer. The width of the resistors is determined by the etching, and the length is determined by the placement of the gold contact pads. Surface resistivities in the order of 400 ohms/square are obtainable, which allows resistor values between 10 ohms and 1,000 ohms to be realized. The final two-stage amplifier is shown in Figure 3.

MEASURED PERFORMANCE

The initial selections of two stage amplifiers were based on DC probing and visual inspection. The amplifiers were further screened by measuring individual FET characteristics such as I_{dss}, V_p, and gm. The chips that were determined "DC good" were then mounted on carrier plates with associated input/output 50 ohm transmission lines fabricated on alumina.

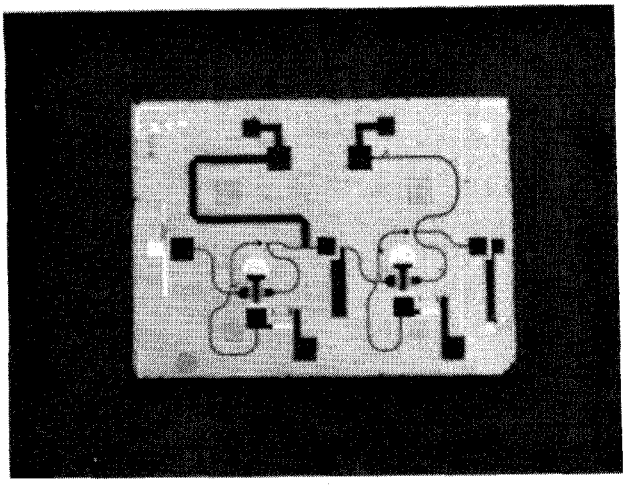

Figure 3. Monolithic two stage amplifier chip.

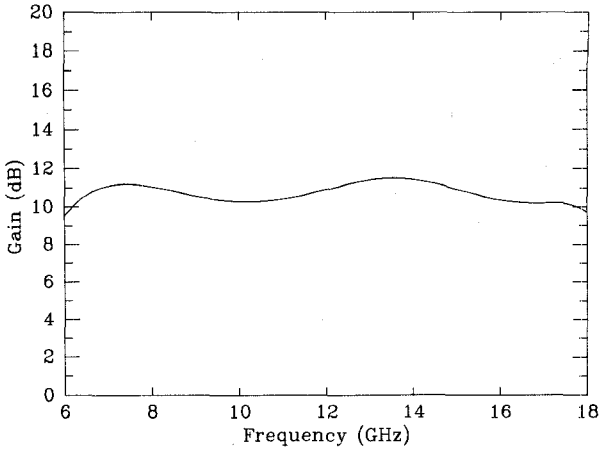

Figure 4. Computed gain performance of modeled two-stage amplifier.

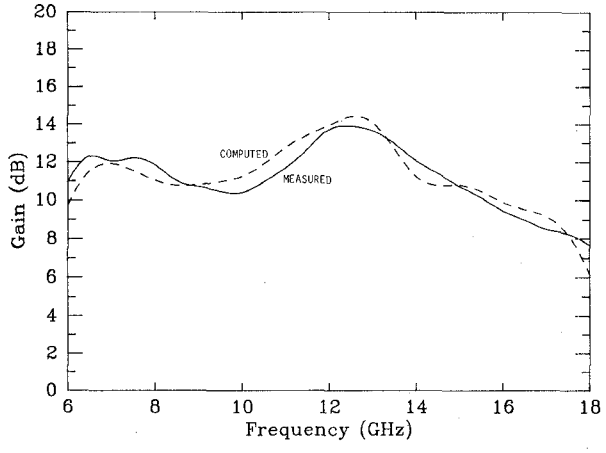

Figure 5. Measured versus computed gain performance using actual circuit and device parameters.

The computed gain performance, which was calculated using circuit and FET models, is shown in Figure 4. The measured gain performance and a new computed response in which the actual values of the feedback resistances and measured FET S-parameters were used in the circuit description, are shown in Figure 5. The difference between the measured and computed gain is due in part to circuit modeling errors and process variations in FET characteristics.

The measured performance indicates that respectable amplifier gain can be obtained at frequencies extending through 18 GHz. It was also found that several two stage amplifiers could be cascaded without any degradation in performance. The noise figure was also measured and is shown in Figure 6.

Although the output network on the amplifier was designed for low VSWR, the FET is terminated so that a modest amount of output power can be obtained. The compression characteristics that are shown in Figure 7, indicate that a minimum output power of 18 dBm is obtainable over the entire frequency range of 6-18 GHz.

CONCLUSION

The illustrated design method allows the microwave engineer to synthesize and analyze broadband monolithic feedback amplifiers. The parasitic elements that degrade ultimate high-frequency performance of feedback amplifiers constructed with hybrid fabrication methods are reduced substantially with monolithic circuit implementations. The resistor lengths and shunt capacitance associated with mounting pads and DC blocking capacitors can be made quite small. Thus, phase shift of the overall loop can also be minimized because it can be placed closer to the active area of the FET than with conventional circuit designs. By properly selecting the device size, the monolithic circuit designer can optimize the input VSWR and the power output capabilities of the resulting amplifier. The excellent stability and impedance control characteristics allow amplifier gain chains to be constructed with cascaded multistage feedback gain blocks, certainly an important factor in reducing the cost, complexity, and size over conventional designs employing cascaded, hybrid-

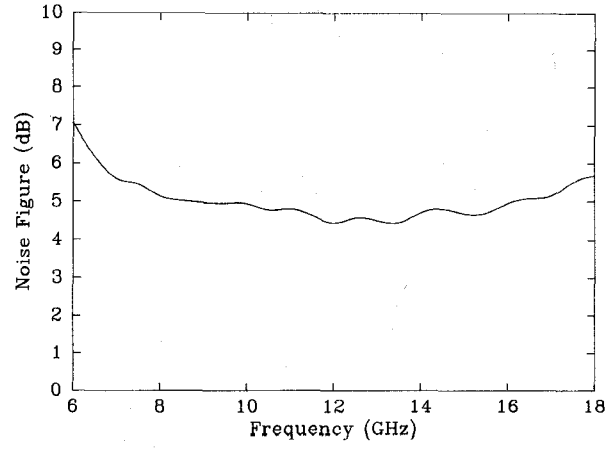

Figure 6. Broadband noise figure of two-stage monolithic amplifier

coupled gain stages. It is hoped that this design method, though more complex than a conventional approach, will aid the microwave engineer in designing stable, single-ended amplifiers, where costly design iterations and balanced configurations are neither desirable nor possible.

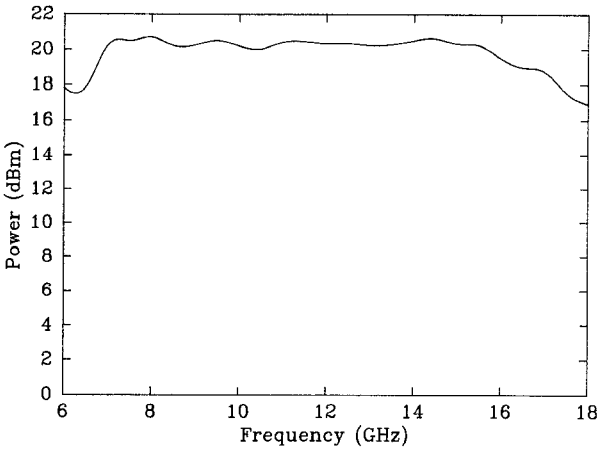

Figure 7. Amplifier power output at 1 dB gain compression point.

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